REMARKS

Applicants respectfully request reconsideration of the application, as amended, in view of the following remarks.

The present invention as set forth in **amended Claim 1** relates to a dielectric separation type semiconductor device, comprising:

a semiconductor substrate;

a primary dielectric layer disposed adjacent to a whole region of a first main surface of said semiconductor substrate;

a first conductivity type first semiconductor layer of a low impurity concentration disposed on a surface of said primary dielectric layer in opposition to said semiconductor substrate so that said primary dielectric layer is sandwiched between said first conductivity type first semiconductor layer and said semiconductor substrate;

a first conductivity type second semiconductor layer of a high impurity concentration formed selectively on the surface of said first semiconductor layer;

a second conductivity type third semiconductor layer of a high impurity concentration disposed so as to surround an outer peripheral edge of said first semiconductor layer with a distance;

a ring-like insulation film disposed so as to surround an outer peripheral edge of said third semiconductor layer;

a first main electrode disposed in contact with a surface of said second semiconductor layer;

a second main electrode disposed in contact with a surface of said third semiconductor layer;

a sheet-like back-surface electrode disposed adjacent to a second main surface of said semiconductor substrate on a side opposite to said first main surf ace of said semiconductor substrate; and

a first auxiliary dielectric layer disposed below said second semiconductor layer, said first auxiliary dielectric layer having a concave shape;

wherein a second auxiliary dielectric layer is disposed between said first auxiliary dielectric layer and said primary dielectric layer; and

wherein said second auxiliary dielectric layer is junctioned to the semiconductor substrate and the first auxiliary dielectric layer.

In contrast, Kobayashi (US 5,476,809) and Akio (JP9-172189) fail to disclose or suggest **a first auxiliary dielectric layer disposed below said second semiconductor layer, said first auxiliary dielectric layer having a concave shape.** See the horizontal part of layer 3 in the Figures of Kobayashi (US 5,476,809) which the Examiner has identified as first auxiliary dielectric layer. See also the abstract and Figures of Akio (JP9-172189).

Therefore, the rejection of Claims 1-4 and 6-7 under 35 U.S.C. § 103(a) as being unpatentable over Kobayashi (US 5,476,809) and Akio (JP9-172189) is believed to be unsustainable as the present invention is neither anticipated nor obvious and withdrawal of this rejection is respectfully requested.

The rejection of Claim 3 under 35 U.S.C. § 112, 2nd paragraph, is obviated by the amendment of Claim 3.

Applicants appreciate the Examiner's indication that the non-elected claims 8-15 will be rejoined once the elected claims have been found allowable.

Applicants respectfully request that the Examiner acknowledge that the references cited in the **Information Disclosure Statement, filed** in the above-identified application on

January 31, 2005, have been considered. For the Examiner's convenience a copy of Form PTO 1449 as filed on January 31, 2005, is attached herewith.

This application presents allowable subject matter, and the Examiner is kindly requested to pass it to issue. Should the Examiner have any questions regarding the claims or otherwise wish to discuss this case, he is kindly invited to contact Applicants' below-signed representative, who would be happy to provide any assistance deemed necessary in speeding this application to allowance.

Respectfully submitted,

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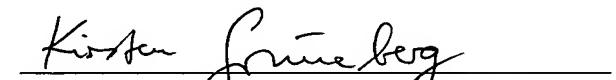

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